DEVELOPMENT OF KEY MONOLITHIC CIRCUITS TO Ka-BAND FULL MMIC RECEIVERS

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ABSTRACT

Key monolithic circuits to Ka-band full MMIC receivers have been designed and fabricated. Conventional hybrid-oriented elements such as RF image-rejection filters, LO dielectric resonators and IF hybrid couplers have been eliminated for the full MMIC configuration. Prospects have been obtained for realization of very-small-size microwave communication receivers.

INTRODUCTION

Microwave communication equipment requires not only high performance but small size and lightweight for air or space applications. Monolithic microwave integrated circuits (MMIC's) have great potential for miniaturization of the equipment. Very-small-size microwave equipment can be realized by applying full MMIC components.

Most practical microwave receivers have been hybrid oriented so far. This is because the constituent hybrid-oriented elements such as image rejection filters and local oscillator resonators are difficult to integrate onto the monolithic semiconductor substrate.

This paper describes the development of key monolithic circuits to Ka-band full MMIC receivers. The heterodyne image signal is canceled by integrated balanced mixers and an active IF hybrid instead of image rejection RF filters. A high-speed PLL stabilizes the local oscillator frequency and reduce the phase noise without high-Q dielectric resonators.

RECEIVER DESIGN

The target of this work is to develop a 30 /1GHz heterodyne down converter with a built-in local oscillator for space-borne receivers in digital satellite communication systems. Receivers for this purpose require both image signal / noise rejection and local frequency stabilization without use of any hybrid circuitry. A possible solution to these requirements is shown in Fig.1. In this receiver configuration, two balanced mixers and an active IF 90° hybrid are employed for image signal / noise rejection. Also employed is a 15GHz PLL oscillator followed by a frequency doubler to obtain a 30GHz stabilized local source. Therefore, the key monolithic circuits to be developed for the receiver are

1) 30GHz RF amplifier
2) 30 / 1GHz balanced mixer
3) 1GHz active IF hybrid
4) 15GHz voltage controlled oscillator
5) 15GHz ÷ 2 frequency divider
6) 15GHz x 2 frequency doubler.

These circuits have been integrated on several pieces of GaAs substrate, and each configuration and achieved performance are discussed in the following chapters.

RF AMPLIFIER

The RF amplifier at this high frequency of 30GHz requires not only broadband performance but also small chip size since the MMIC package must be small enough to prevent waveguide-

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mode package resonances. Lumped-constant MIM (Metal-Insulator-Metal) capacitors provide more broadband and compact matching networks than the conventional distributed-constant microstrip stub lines. However, the MIM capacitors have much deviation in its capacitance owing to the fabricated insulator thickness deviation. Therefore, this RF amplifier has been designed by employing a novel circuit configuration compensating the parameter deviation of the MIM capacitors as shown in Fig.2. A 30GHz band two-stage FET amplifier with the input / output matching networks has been integrated in a 2×3.5×0.15mm GaAs chip. A typical gain more than 4dB / chip has been obtained in the frequency range of 27-30 GHz as shown in Fig.3. A gain deviation has been within ±0.5dB for most fabricated chips.

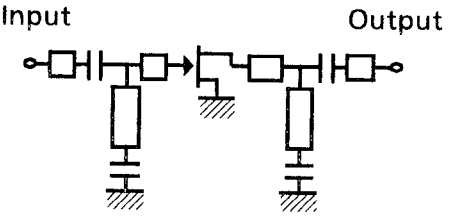

Fig.2 - RF amplifier circuit diagram

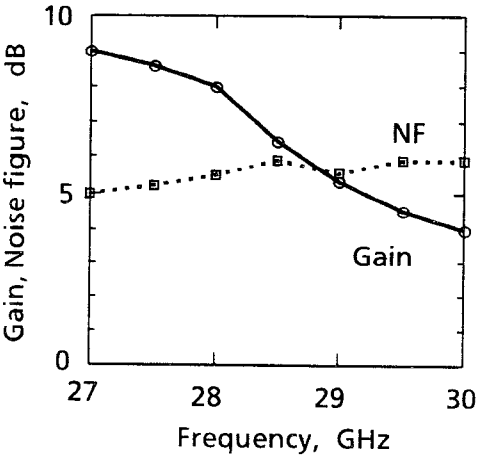

Fig.3 - RF amplifier gain and noise

BALANCED MIXERS

Since the RF amplifier has broadband response, undesired image signals / noise may be received or generated in the RF amplifier. In order to cancel these undesired images, two balanced mixers have

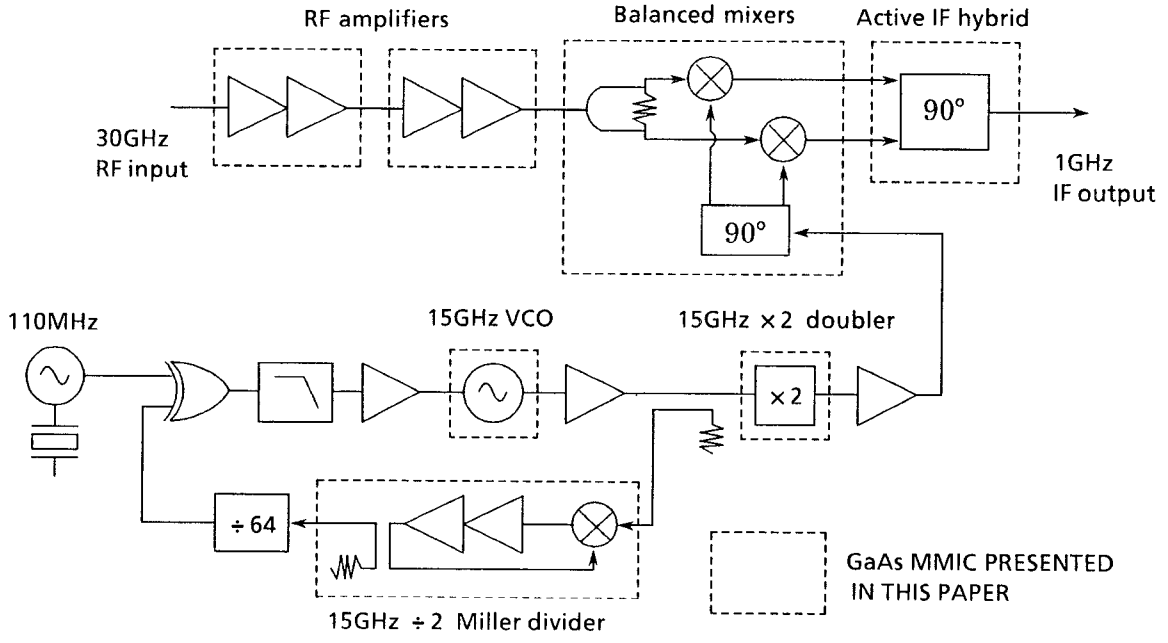

Fig.1 - Ka-band full MMIC receiver block diagram

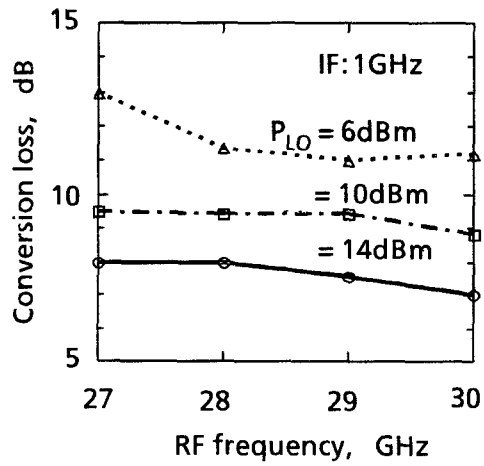

Fig.4 - Balanced mixer conversion loss

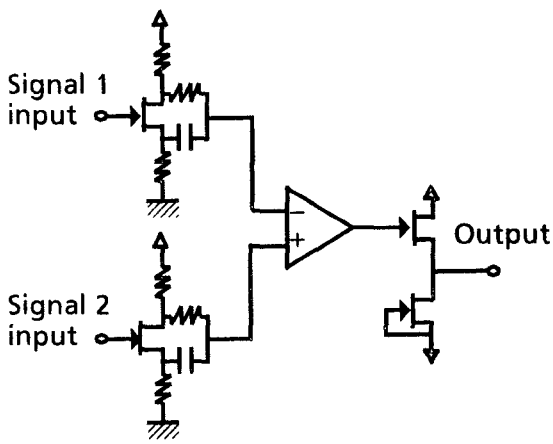

Fig.5 - Active hybrid circuit diagram

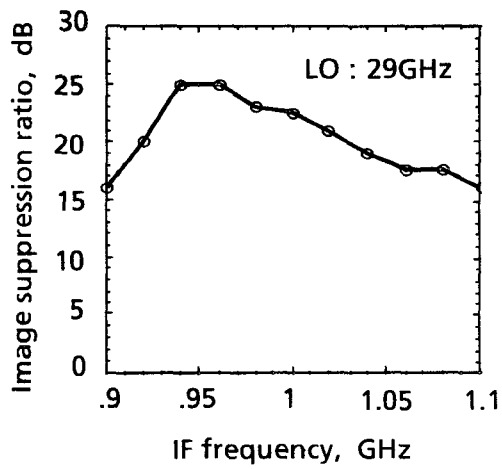

Fig.6 -.Image rejection performance

been adopted and coupled with an RF power divider and an LO branch-line coupler. Each balanced mixer has been composed of another branch-line coupler and a pair of Schottky diodes with impedance matching networks for wide band mixer operation. Those circuits have been integrated in a 4.2×3.5×0.15mm GaAs chip. The each balanced mixer can operate in a broadband frequency range of 27-30GHz with less than 8dB conversion loss, as shown in Fig.4. The image cancellation is carried out by these mixers and an active IF hybrid as discussed in the next two chapters.

ACTIVE IF HYBRID

In the IF band of 1GHz, the quarter wavelength exceeds the maximum chip size practically available. Since the conventional passive branch-line 90° hybrid does not match the full MMIC configuration, an active IF hybrid has been designed. It consists of two FET-CR phase shifters with constant-amplitude characteristics as shown in Fig.5. The two input IF signals are combined under the constant phase difference of 90 degrees. This active hybrid, including no distributed-constant elements, has been integrated in a 1.5×3.5×0.15mm GaAs chip. Almost constant phase-frequency characteristics have been obtained in the 0.5-1.5GHz IF range within ±5 degree phase deviation.

CANCELLATION OF IMAGE SIGNALS

The above described two balanced mixers and the active IF hybrid have been linked so as to confirm the cancellation of images. An RF signal and undesired images are fed in phase into the two mixers via a 3dB power splitter. Since the two mixers are pumped by orthogonal local signals, the output images from the two mixers cancel each other. A total signal-to-image ratio of 15 - 25dB has been obtained as shown in Fig.6.

VOLTAGE CONTROLLED OSCILLATOR

Monolithic circuits have fairly low Q factors, resulting in MMIC oscillators with parasitic

oscillations. The oscillation frequency is susceptible to the device parameters and the load impedance. Moreover, frequency trimming is difficult to carry out after fabricating an MMIC. Therefore, circuits must be designed taking tuning ranges and pulling figures into account[1].

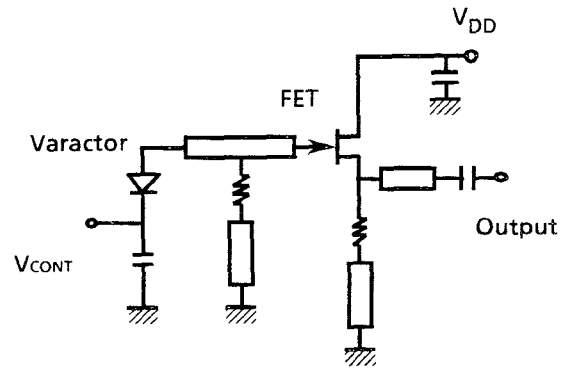

Fig.7 - VCO circuit diagram

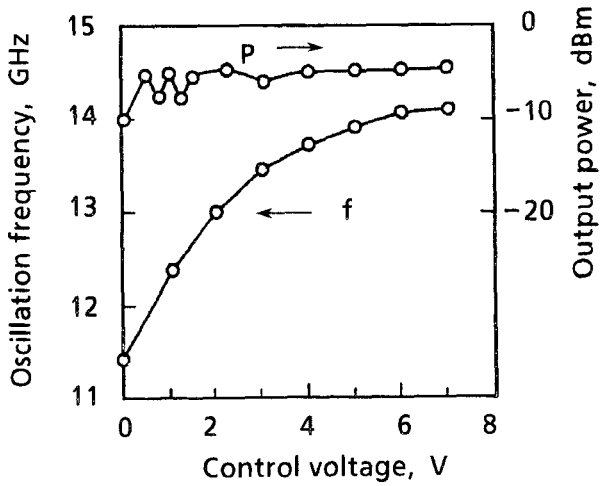

Fig.8 - VCO tuning characteristics

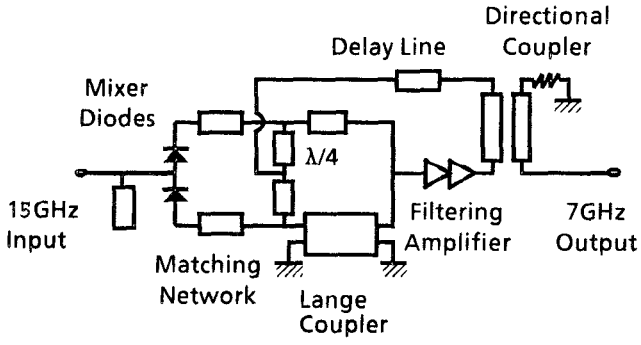

Fig.9 - Miller frequency divider circuit diagram

The VCO developed here employs the source-follower common-drain circuit to obtain wider tuning range and lower pulling figure. To prevent parasitic oscillation, a novel out-of-band dumping circuit has been used in the impedance matching network as shown in Fig.7.

The VCO has been implemented in a 2×2×0.15mm GaAs chip. It has tuned smoothly from 11.3GHz to 14.3GHz by the control voltage on the varactor diode as shown in Fig.8. No parasitic oscillation has been found in the observed throughout the frequency range of DC-22GHz.

MILLER FREQUENCY DIVIDER

A regenerative frequency divider was proposed by Miller[2]. The divider is a down converter with a feedback loop consisting of a balanced mixer and a filtering amplifier. It operates much faster than conventional digital frequency dividers. The MMIC implementation of the Miller frequency divider shown in Fig.9 has already been reported by the authors[3]. The prototype MMIC Miller frequency divider is employed here as a key circuit in the phase-locked loop.

Before applying the developed divider to the PLL, the divider characteristic has been measured and analyzed in terms of input-to-output phase noise performance. The measured input-to-output phase noise SSB power density is depicted in

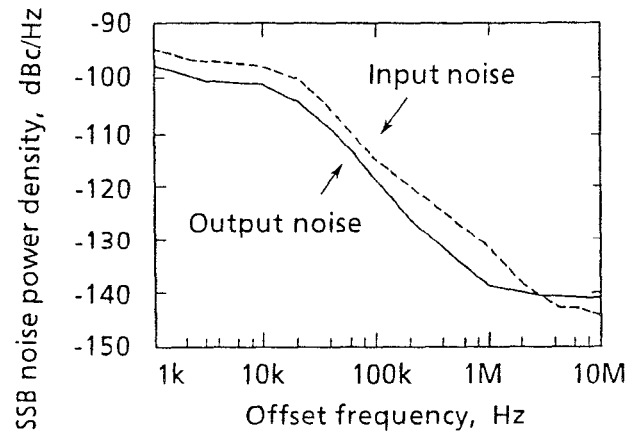

Fig.10 - Miller frequency divider phase noise

Fig.10. The resultant data show that the output noise is 4 - 8dB lower than the input noise. This agrees fairly well with the theoretical prediction[4].

PHASE NOISE REDUCTION

The MMIC VCO is widely tunable but has a fairly blunt or noisy spectrum due to its low-Q property. The oscillation phase noise comes from the quick fluctuation in the oscillation frequency. The PLL technique presented here is based on a theory, in which the quick fluctuation is suppressed significantly by high-speed tracking and control of the VCO. The loop parameters have been determined so that the loop bandwidth might be much wider and time delay in loop might be much smaller than conventional high-Q oscillators.

The above mentioned MMIC VCO and Miller frequency divider have been assembled into a PLL local oscillator shown in Fig.1. The measured oscillation phase noise is depicted in Fig.11. Increasing the loop gain K up to 5×10^6 [s^{-1}], the SSB noise power density is reduced to less than -80dBc / Hz at 1kHz off from the carrier. Spectral purity quite equal to reference crystal oscillator has been obtained.

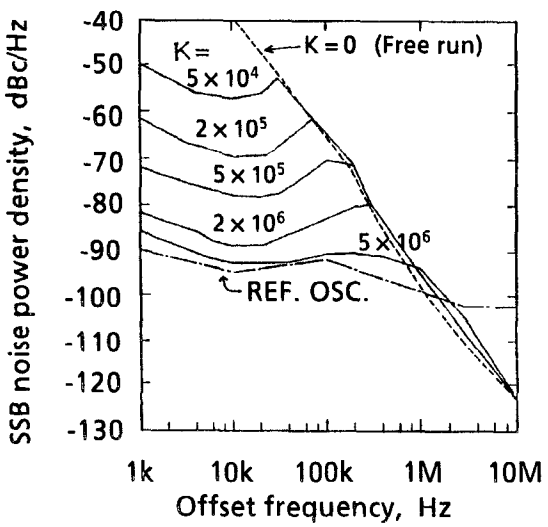

Fig.11 - Phase noise reduction by high-speed PLL

FREQUENCY DOUBLER

An FET doubler is expected to have a frequency response broader than that of varactor-diode doublers. The main difficulties in FET doubler design, however, are (1) estimation of input / output matching impedance of the FET in the nonlinear operation, (2) design of the output matching network which transmits the second harmonic wave and reflects the fundamental wave.

Since nonlinear S parameters of FET's are difficult to measure directly, a practical method for determining the parameters has been incorporated. This measuring method is based upon the principle that the optimum matching impedance is equal to the device parameter conjugate. By this method, the FET doubler has been designed and integrated in a 2.5x2x0.15mm GaAs chip. Conversion loss less than 5dB and fundamental-wave suppression more than 10dB have been obtained in the wide frequency range shown in Fig.12.

CONCLUSIONS

Key monolithic circuits to Ka-band full MMIC receivers have been developed. Heterodyne image rejection ratio of 15 - 25dB has been obtained at the 30GHz band by use of integrated balanced mixers and an active IF hybrid. A high-speed PLL

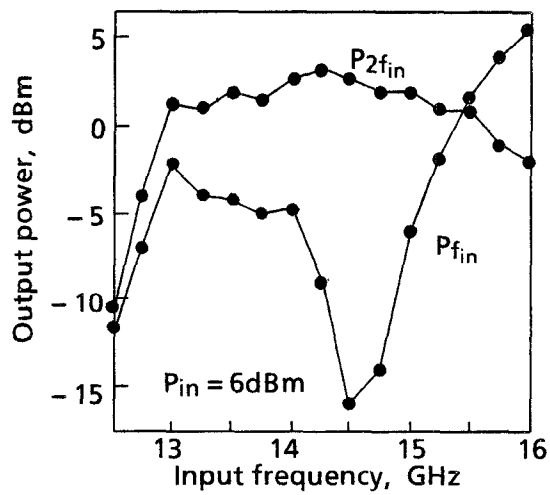

Fig.12 - Frequency doubler frequency response

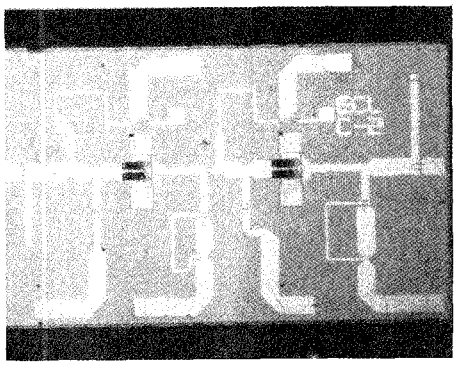

Fig.13 - 30GHz RF amplifier

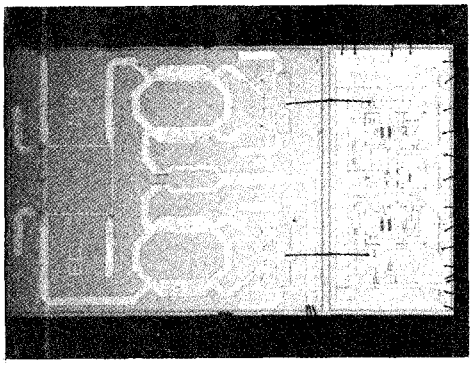

Fig.14 - Balanced mixers with active IF hybrid

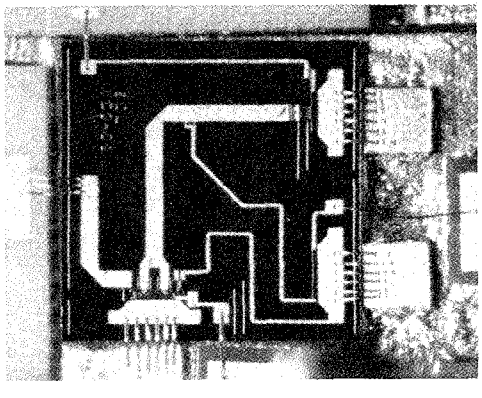

Fig 15 - 15GHz VCO

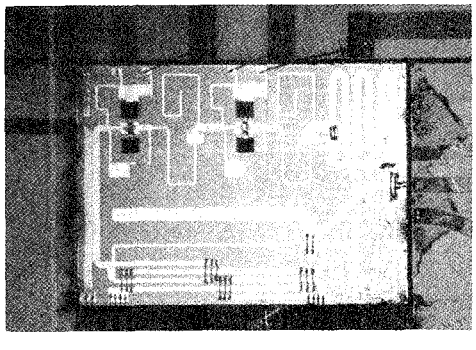

Fig 16 - 15 / 7GHz Miller frequency divider

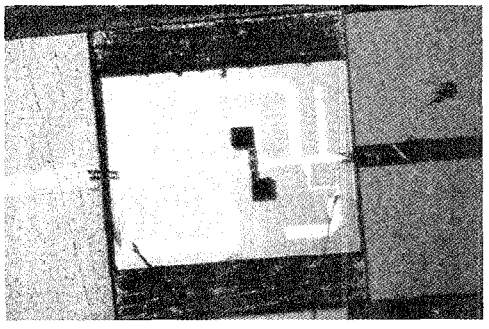

Fig 17 - 15 / 30GHz frequency doubler

has reduced the oscillation phase noise into -80dB / Hz at 1kHz offset from carrier. This study has shown that full MMIC receivers can be realized without high-Q filters or resonators.

Applying this MMIC technology, a complete receiver module with associate circuitry can be reduced to 1/2 - 1/3 in its weight. For further weight reduction of practical onboard receivers, miniaturization of peripheral constituents such as dc voltage converter and housing case is expected and this will enhance the lightweight performance of the full MMIC configuration.

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